DERWENT-ACC-NO: 2004-287378

DERWENT-WEEK: 200427

TITLE: Semiconductor memory e.g. metal oxide nitride oxide semiconductor memory has one pair of insulating layers with nitridation films, that are formed so that control gates and another pair of layers formed on gates, are covered

PATENT-ASSIGNEE: SEIKO EPSON CORP[SHIH]

PRIORITY-DATA: 2002JP-0223708 (July 31, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2004064012 A	February 26, 2004	N/A	022	H01L 021/8247

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP2004064012A	N/A	2002JP-0223708	July 31, 2002

INT-CL (IPC): H01L021/8234, H01L021/8247 , H01L027/088 , H01L027/10 , H01L027/115 , H01L029/788 , H01L029/792

ABSTRACTED-PUB-NO: JP2004064012A

BASIC-ABSTRACT:

NOVELTY - The control gates (20,30) are formed at both sides of a word gate (14) formed on a substrate (10) through oxide nitride-oxide (ONO) films. One pair of sidewall insulating layers (52) is formed at upper portions of the control gates. Another pair of sidewall insulating layers (54) with nitridation films, is formed at the sides of the gates so that the control gates and the insulating layers (52) are covered.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing
method of semiconductor memory.

USE - Semiconductor memory e.g. metal oxide nitride oxide semiconductor (MONOS) memory and silicon oxide nitride oxide semiconductor (SONOS) memory.

ADVANTAGE - Prevents exposure of natural oxidation film, before silicide formation, by forming sidewall insulating layer with nitridation film.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the semiconductor memory.

semiconductor substrate 10

gate insulating layer 12

word gate 14

impurity layers 16,18

control gates 20,30

sidewall insulating layers 50,52,54

memory cell 100

metal oxide semiconductor transistor 500

memory range 1000

logic circuit range 2000

CHOSEN-DRAWING: Dwg.3/19

TITLE-TERMS: SEMICONDUCTOR MEMORY METAL OXIDE NITRIDE OXIDE SEMICONDUCTOR
MEMORY ONE PAIR INSULATE LAYER NITRIDATION FILM FORMING SO CONTROL
GATE PAIR LAYER FORMING GATE COVER

DERWENT-CLASS: L03 U11 U14

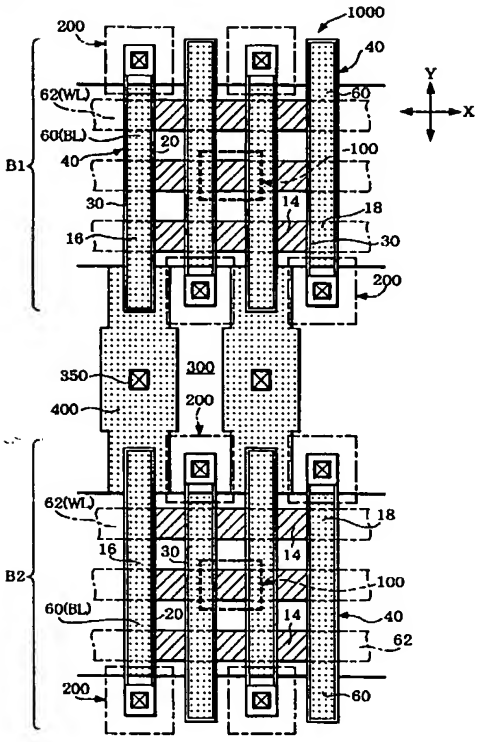
CPI-CODES: L04-C11C1; L04-C12A; L04-C12B;

EPI-CODES: U11-C05B5; U11-C05F1; U14-A03B7;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2004-110861
Non-CPI Secondary Accession Numbers: N2004-227951

８０　配線層
１００　不揮発性記憶装置（メモリセル）
１２０　絶縁層
１２２　第３ゲート絶縁層
１４０，１４０ａ，１４０ｂ　ゲート層
１４２　ゲート電極
１６０，１８０　開口部
１６２，１８２　不純物層
２７０　絶縁層
３００　素子分離領域
４００　コンタクト用不純物層
５００　絶縁ゲート電界効果トランジスタ（ＭＯＳトランジスタ）
Ｓ１００　ストッパ層
Ｒ１００、Ｒ２００、Ｒ３００　レジスト層
１０００　メモリ領域
２０００　ロジック回路領域

【図１】



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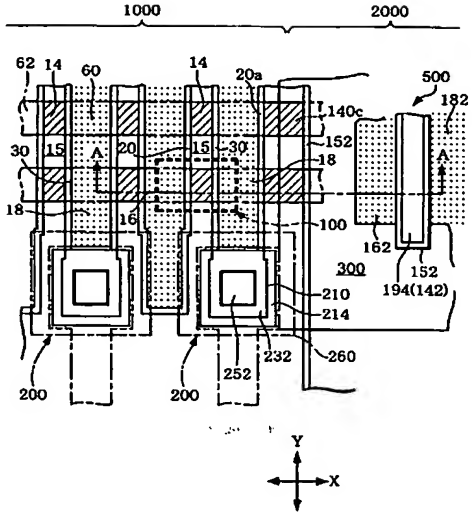

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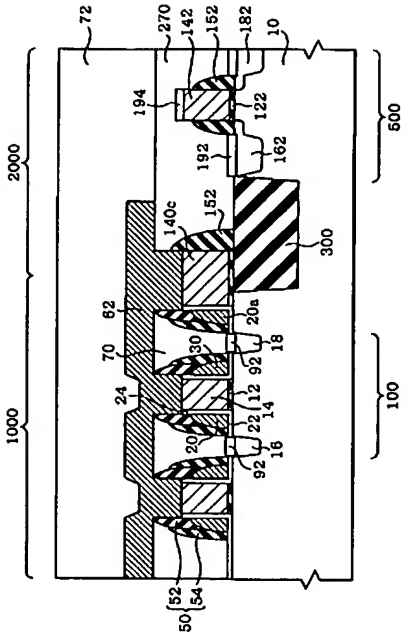
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152
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62
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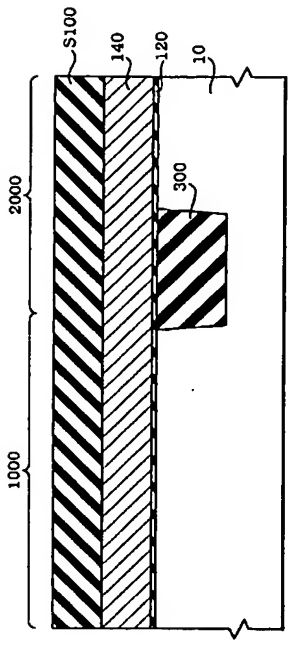
12
14
22
20
16
92
100
1000
52
54
50

【図４】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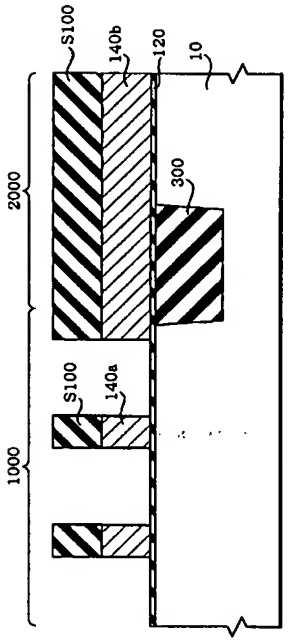
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120
10
2000
300
S100
140a
1000

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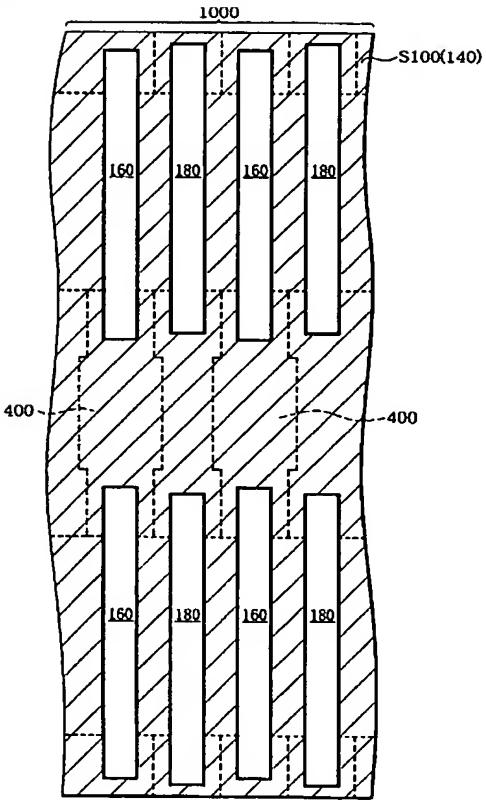
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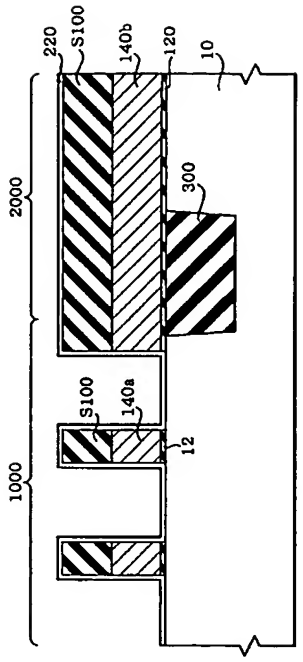
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12
1000

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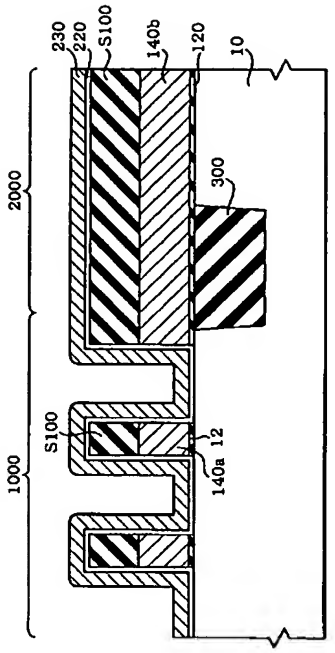
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S100
140a
12
1000

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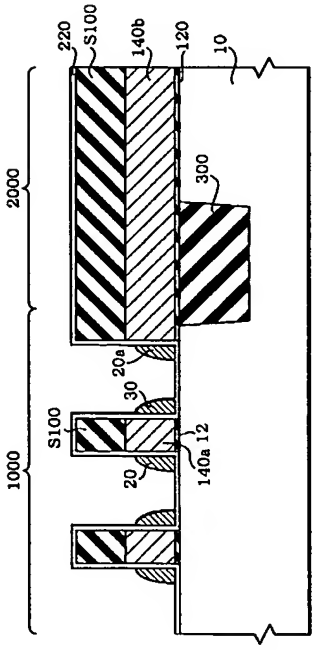
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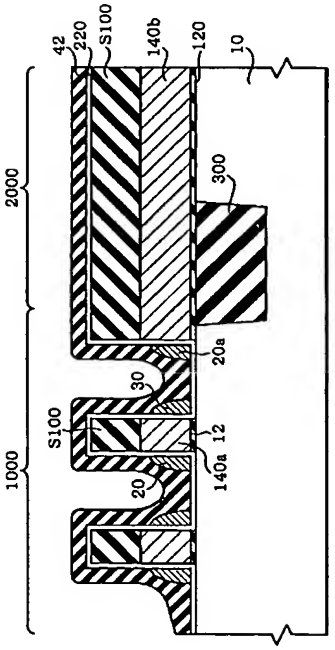
S100
140a
12
20
1000

【図１０】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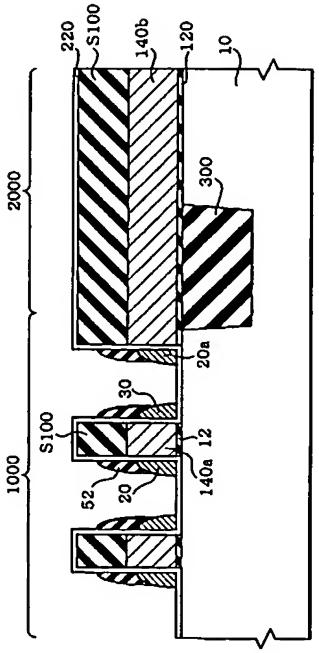
S100
140a
12
20
1000

【図１１】



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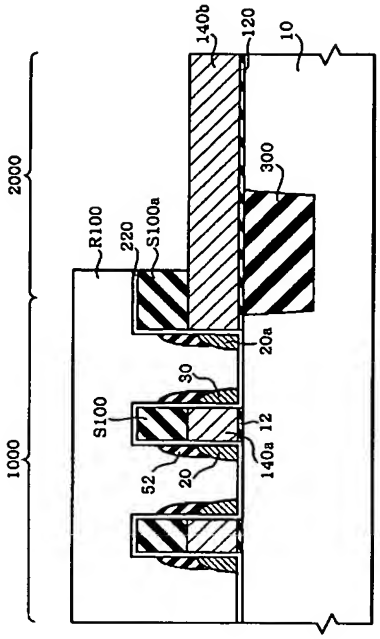

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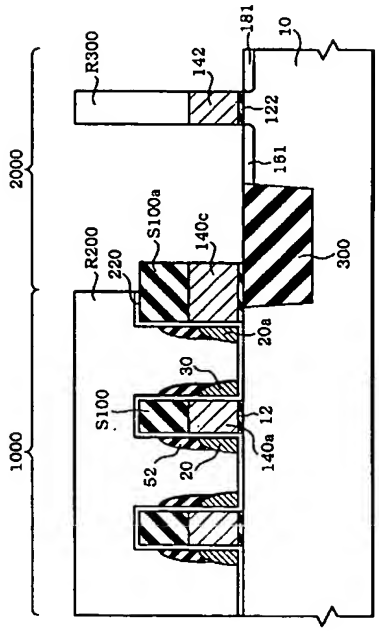

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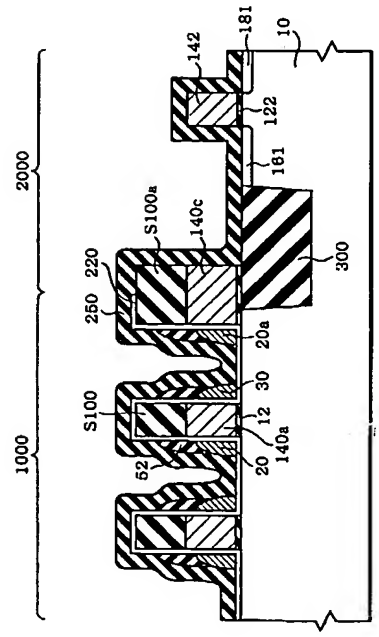

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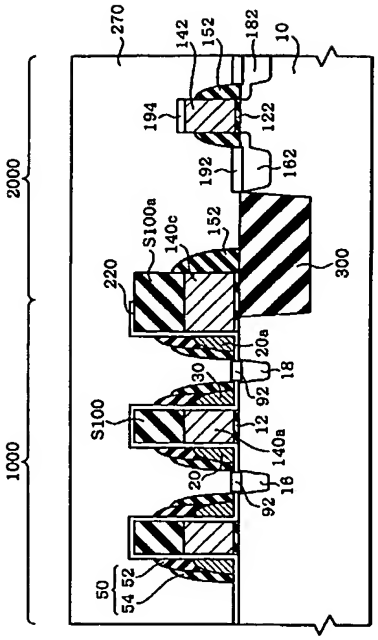

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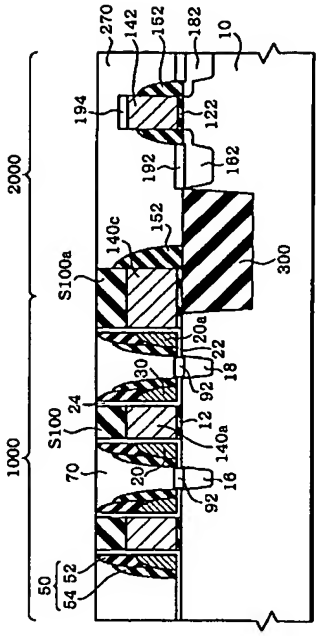

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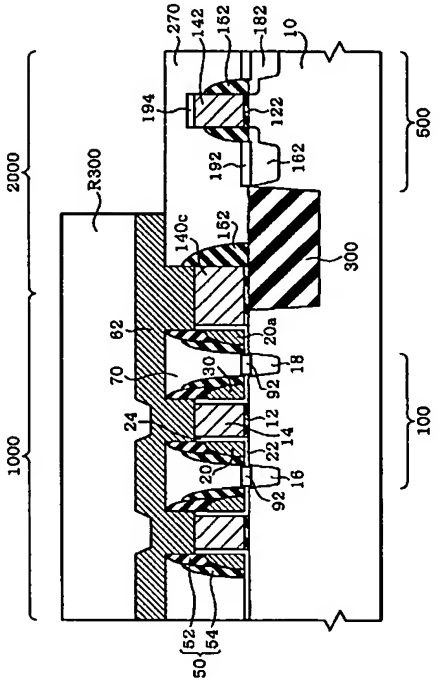

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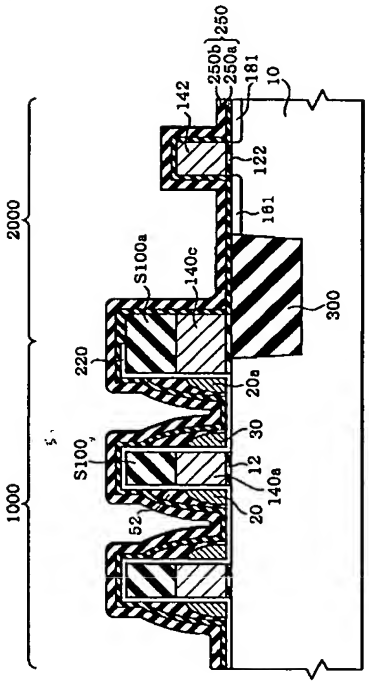

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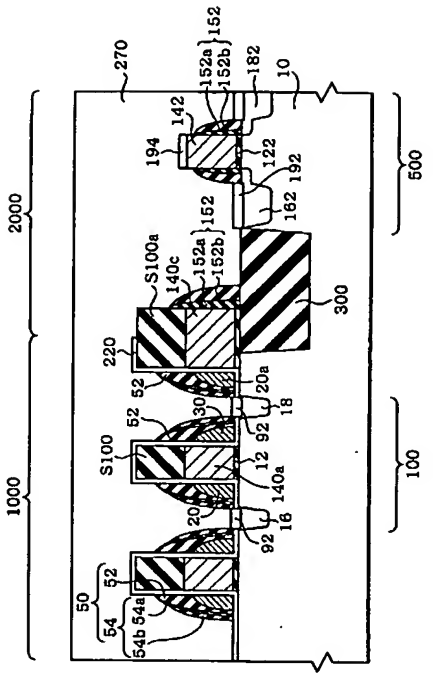
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S100a
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300
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20a
18
30
52
S100
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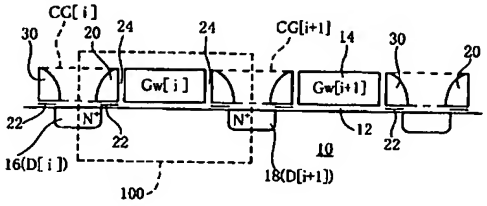
16
92
52
50
54
54a
54b

【図２０】


CG[i]
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24
24
CG[i+1]
14
30
20
Gw[i]
Gw[i+1]
22
N+
N+
22
12
22
10
16(D[i])
18(D[i+1])
100